<u>IN THE SPECIFICATION</u>:

Please amend paragraph number **[0001]** as follows:

[0001] ~~Cross Reference~~ <u>Cross-Reference</u> to Related Application: This application is a continuation of application Serial No. 08/814,900, filed March ~~12,~~ <u>21,</u> 1997, ~~pending.~~ <u>now U.S. Patent 6,350,322, issued February 26, 2002.</u>

Please amend paragraph number **[0014]** as follows:

[0014] In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel for a chemical treatment. Following the chemical treatment, the semiconductor structure is transferred directly from the first treatment vessel to a second treatment vessel. The semiconductor structure is rinsed with DI water in the second treatment vessel. Next, the second treatment vessel is flooded with DI water to form a DI water bath. The second treatment vessel may also be optionally flooded with a gas that is inert to the ambient, such as nitrogen, to form <u>an inert atmosphere</u> in the second treatment vessel ~~an inert atmosphere~~. The inert gas forming the inert atmosphere is intended herein to mean a gas that does not substantially react with or otherwise contaminate the semiconductor structure or the vessel in which the inert atmosphere is formed under the processing conditions set forth herein. The inert atmosphere is maintained during rinsing. Following rinsing, a gaseous stream, such as nitrogen, that is laden with IPA vapor is fed into the second treatment vessel.

Please amend paragraph number **[0017]** as follows:

[0017] In a third embodiment of the present invention, a rinser is ~~retrofit~~ <u>retrofitted</u> with a lid and a fail-shut valve. In the third embodiment, the process of chemical treatment is carried out conventionally, but DI water rinsing and drying both occur within the rinser. Following sufficient rinse cycles, IPA-laden nitrogen is fed into the rinser in a manner similar to the method of the second embodiment. Entrainment of substantially all DI water, and contaminants therein, beneath the IPA layer is accomplished by displacement of the last spray/dump DI water volume with an IPA-DI water interface as set forth above. In this

embodiment, ~~retrofit~~ retrofitted rinsers include spray/dump rinsers, overflow rinsers, cascade rinsers, and Marangoni dryers that have been ~~retrofit~~ retrofitted with rinsing capabilities.

Please amend paragraph number **[0019]** as follows:

[0019] In order ~~that the manner in which~~ to obtain the above-recited and other advantages of the invention ~~are obtained~~, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are ~~not therefore~~ not, therefore, to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Please amend paragraph number **[0029]** as follows:

[0029] Rinsing by the method of the present invention is usually carried out with DI water. Other rinsing solutions may be used such as aqueous hydrogen peroxide. Drying by the method of the present invention comprises forming a substantially continuous layer of a drying liquid upon the upper surface of a DI water bath in which the semiconductor structure is submerged. Following formation of the substantially continuous layer of the drying liquid, the semiconductor structure is drawn through the substantially continuous layer of the drying liquid. Both the DI water and contaminants therein are entrained beneath the substantially continuous layer of the drying liquid in the DI water bath and ~~are therefore~~ are, therefore, substantially removed from the semiconductor structure.

Please amend paragraph number **[0030]** as follows:

[0030] The drying liquid comprises a volatile liquid such as IPA. Other drying liquids are contemplated to be, but need not be, derived from an anhydrous organic vapor, such as acetone, chloroform, methanol, carbon tetrachloride, benzene, ethanol, ethyl acetate, hexane, ~~1-propanol,~~ 1-propanol, and 2-propanol, and equivalents. By reading the disclosure of the present

invention and by practicing the present invention, one of ordinary skill in the art will recognize that anhydrous organic liquids or the like may be used in the method of the present invention. The skilled practitioner will recognize that, although a water-miscible drying liquid such as IPA may be used, such liquids are preferred to be more volatile than the DI water used for rinsing, and such liquids are preferred in that they are not prone to cause deleterious chemical effects upon the semiconductor structure.

Please amend paragraph number **[0032]** as follows:

[0032] In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Chemical treatment may be any number of treatments such as rinsing the semiconductor structure in an aqueous HF solution, performing an HF dry etch on the semiconductor structure, performing a buffered oxide etch on the semiconductor structure, performing a polysilicon etch on the semiconductor structure, other wet or dry etching processes, photoresist stripping, or RCA cleaning. In an example of the first embodiment, an HF rinse is carried out in which aqueous HF contacts the semiconductor structure and is optionally filtered and recirculated. The aqueous HF is discarded after a number of ~~uses~~ uses, depending upon the specific application.

Please amend paragraph number **[0033]** as follows:

[0033] Following the chemical treatment step, a rinsing step is carried out usually by transferring the semiconductor structure to a second treatment vessel and performing a DI water rinse. DI water rinsing vessels are known in the art such as a cascade rinser, an overflow rinser, a spray/dump rinser, a spin/rinse dryer, an etcher/rinser, and others. In the first embodiment of the present invention, the rinsing vessel is omitted. The semiconductor structure is transferred directly from the first treatment vessel to a second treatment vessel, rinsed in the second treatment vessel, and then dried. In this first embodiment of the present invention, the semiconductor structure is transferred from an HF-last cleaning vessel to a Marangoni dryer that

has been ~~retrofit~~ retrofitted with means for contacting the semiconductor structure with DI water, such as with spray nozzles for rinsing the semiconductor structure.

Please amend paragraph number **[0034]** as follows:

[0034] In the first example of the first embodiment of the present invention, most of the hydrophobic surfaces of the semiconductor structure are hydrogen terminated, ~~e.g.~~ *e.g.*, M-H, where M represents Si, Al, Al alloys, and other metals. About ten to twenty percent of the bonds, however, are M-F instead of the preferred M-H. Because significant oxidation occurs only after the rinsing, and because significant water spotting occurs only during spin drying or post-rinse (pre-dry) atmospheric exposure, exposing the semiconductor structure to the ambient by transferring it from an HF rinsing treatment vessel to a rinse/dry treatment vessel under conventional clean room conditions results in some contamination of the semiconductor structure. The inventive method, therefore, does not expose the semiconductor structure to ambient air after rinsing.

Please amend paragraph number **[0036]** as follows:

[0036] Rinsing is commenced within the second treatment vessel. Following appropriate rinsing, the second treatment vessel is optionally cleaned and a DI water bath is formed in the second treatment vessel. A nitrogen stream that is laden with IPA vapor is fed into the second treatment vessel. Alternatively, an IPA stream with no nitrogen or other inert gas acting as a carrier is fed to the second treatment vessel. After a preferred period of time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. When a sufficient layer of IPA vapor has formed upon the surface of the DI water bath, the semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, on the semiconductor structure to be entrained beneath the ~~IPA-DI~~ IPA-DI water interface. Impurities in the DI water bath are substantially all retained in the DI water bath as the semiconductor structure is drawn through the IPA-DI water interface. By this method, unwanted oxidation incident to ambient exposure of the semiconductor structure is

minimized, and unwanted water spotting incident to spin drying and ~~incident to post rinse~~ to post-rinse atmospheric exposure is eliminated.

Please amend paragraph number **[0042]** as follows:

[0042] Check valve 18 can be configured within valve housing 26 such that a selected clearance 22 limits how high ball 28 of check valve 18 may ~~rise, and therefore~~ rise and, therefore, how large an effluent opening allows effluent flow F to pass through. It can be seen in FIG. 2 that clearance 22 could be configured to allow ball 28 of check valve 18 to move less than one diameter thereof, or to move greater than one diameter thereof. It will be appreciated by one of ordinary skill in the art that using the present disclosure as a guide, clearance 22 may be adjusted within a single valve housing by placing a screw or piston above ball 28 of check valve 18 to adjustably limit its upward motion.

Please amend paragraph number **[0045]** as follows:

[0045] The process of entraining DI water and thereby substantially removing DI water, and contaminants therein, from the semiconductor structure by the method of the present invention may be accomplished in the second embodiment by a rapid displacement of the DI water bath such that the IPA layer "wipes down" the semiconductor structure in a substantially continuous stroke. A rapid displacement may be accomplished, for example, by pushing ~~IPA-laden~~ IPA-laden nitrogen from a piston that displaces a volume approximately equal to the volume of the gas etch chamber.

Please amend paragraph number **[0047]** as follows:

[0047] A third embodiment of the present invention comprises a ~~retrofit~~ retrofitted spray/dump rinser 32 with a rinser-sealable lid 54 and a valve 34 such as those depicted in FIGS. 4-6. In the third embodiment, the process of chemical treatment is carried out conventionally, but DI water rinsing and drying both occur within the rinser. Following sufficient spray/dump cycles, ~~IPA-laden~~ IPA-laden nitrogen or the like is fed into the rinser in a manner similar to the method of the

second embodiment of the present invention. Removal of DI water from the semiconductor structure comprises displacement of the last spray/dump DI water volume by forming an IPA-DI water interface as set forth above.

Please amend paragraph number **[0048]** as follows:

[0048] The artisan will appreciate that other rinsers may be ~~retrofit~~ retrofitted to practice the method of the present invention. For example, an overflow rinser or a cascade rinser may be ~~retrofit,~~ retrofitted, as well as spinner rinser/dryers. FIG. 5 illustrates an elevational side view of an overflow rinser 40 that has been ~~retrofit~~ retrofitted with a rinser-sealable lid 54, a vapor-gas inlet 52, a semiconductor structure holder 50, and at least one fail-shut valve 34 or a goose neck. During the process of passing an IPA-DI water interface across a semiconductor structure 56, IPA-laden nitrogen gas or the like is fed through vapor-gas inlet 52 while influent DI water that normally enters from below overflow rinser 40 is shut off.

Please amend paragraph number **[0049]** as follows:

[0049] FIG. 6 illustrates an elevational side view of a ~~retrofit~~ retrofitted cascade rinser 42 in which semiconductor structure 56 is substantially batch treated instead of counter-current treated. Influent DI water flows in the direction F and spills over weirs 48. After sufficient rinsing, such that semiconductor structure 56 contacted with the DI water that is about to exit cascade rinser 42 is substantially as thoroughly rinsed as semiconductor structure 56 contacted with the first influent DI water, influent DI water is shut off and IPA-laden nitrogen gas or the like is fed through vapor-gas inlet 52. Fail-shut valves 34 are opened and the pressure of influent ~~IPA-laden~~ IPA-laden nitrogen gas that is fed through vapor-gas inlet 52 displaces all DI water contained within cascade rinser 42.

Please amend paragraph number **[0050]** as follows:

[0050] Draining each stage in cascade rinser 42 may require that fail-shut valve 34 in the deepest stage ~~needs to open~~ be opened first. DI water then drains from the deepest stage

until the DI water depth in the deepest stage matches that of the next deepest stage, at which point fail-shut valve 34 in that stage opens, and so forth for each stage.

Please amend paragraph number **[0052]** as follows:

[0052] FIG. 7 illustrates an elevational side view of a spray/dump rinser 38 that has been ~~retrofit~~ retrofitted with rinser-sealable lid 54 and vapor-gas inlet 52. In the method of the present invention, the normal spray/dump cycle is carried out in an inert atmosphere that may be supplied through vapor-gas inlet 52. The final flooding of spray/dump rinser 38 comprises forming an IPA layer upon the DI water bath and either drawing semiconductor structure 56 through the IPA surface or draining the DI water bath as set forth above such that the IPA surface passes across semiconductor structure 56.